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EXAMINER	
THANGAVELU, KANDASAMY	
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Please find below and/or attached an Office communication concerning this application or proceeding.

PRG

Office Action Summary	Application No. 09/580,854	Applicant(s) SIRICHOTIYAKUL ET AL.
	Examiner Kandasamy Thangavelu	Art Unit 2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 05 January 2004.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-29 and 31-44 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-29 and 31-44 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 30 May 2000 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is in response to the Applicants' Response mailed on January 5, 2004. Claims 21, 39, 40 and 43 were amended. Claims 1-29 and 31-43 of the application are pending. This office action is made non-final.

Response to Arguments

2. Applicants' amendments filed on January 5, 2004 have been fully considered. Additional claim rejections under 35 USC 112 Second Paragraph, 35 USC 101 and 35 USC 102 (a) are included in this office action in response to claim amendments.

Drawings

3. The drawings submitted on May 30, 2000 are accepted.

Claim Rejections - 35 USC § 101

4. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claims 1- 29 and 31-40 are rejected under 35 U.S.C. 101 because the claimed inventions are directed to non-statutory subject matter.

Independent claim 1 recites a mathematical algorithm for determining a dominant logic state, which consists of partitioning an integrated circuit, determining a partial logic state, modifying the representation and determining the dominant logic state. A mathematical algorithm is not statutory subject matter.

Dependent claims 2-11 depend on Claim 1 but do not add further statutory steps.

Independent claim 12 recites a mathematical algorithm for determining a leakage current of an integrated circuit, which consists of partitioning an integrated circuit, determining the dominant logic state and calculating a leakage current. A mathematical algorithm is not statutory subject matter.

Dependent claims 13-20 depend on Claim 12 but do not add further statutory steps.

Independent claim 21 recites a mathematical algorithm for improving the performance of an integrated circuit, which consists of partitioning an integrated circuit, determining the dominant logic state, calculating a leakage current, setting selected one of transistors to a second threshold voltage and modifying the area of transistors. A mathematical algorithm is not statutory subject matter.

Dependent claims 22-29 depend on Claim 21 but do not add further statutory steps.

Independent claim 32 recites a mathematical algorithm for determining a leakage current of an integrated circuit, which consists of constructing a graph of an integrated circuit, calculating a leakage current for each transistor, modifying the graph and calculating a leakage current for a second set of transistors. A mathematical algorithm is not statutory subject matter.

Dependent claims 33-40 depend on Claim 12 but do not add further statutory steps.

6. Claims 1- 29 and 31-40 would be allowable if they are written as a computer implemented method for determining dominant logic state of an integrated circuit, for determining a leakage current of an integrated circuit, for improving the performance of an integrated circuit, or for determining a leakage current of an integrated circuit comprising the steps of ....

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. § 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 32 is rejected under 35 U.S.C. § 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted steps are:

partitioning the integrated circuit into at least one DC-connected component (DCC);

determining a dominant logic state corresponding to the at least one DCC.

Claim 44 is rejected under 35 U.S.C. § 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are:

a plurality of instructions for partitioning the integrated circuit into at least one DC-connected component (DCC); and

a plurality of instructions for determining a dominant logic state corresponding to the at least one DCC.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

9. Claims 1-29 and 31-44 are rejected under 35 U.S.C. § 102(a) as being anticipated by **Sirichotiyakul et al. (SI)** ("Stand-by power minimization through simultaneous threshold voltage selection and circuit sizing", ACM 1999).

9.1 **SI** teaches Stand-by power minimization through simultaneous threshold voltage selection and circuit sizing. Specifically, as per claim 1, **SI** teaches a method for determining a dominant logic state in an integrated circuit (Page 437, CL2, Para 1 and CL2, Para 4); comprising:

using a representation of the integrated circuit to determine a first partition and a second partition wherein the first partition includes a first power supply node and the second partition

includes a second power supply node (Page 438, CL1, Fig 2; CL2, Fig 3; CL1, Para 3; CL2, Para 2);

determining a partial logic state corresponding to the first and second partitions (Page 438, CL1, Fig 2; CL2, Para 7);

modifying the representation according to the partial logic state (Page 438, CL2, Para 7); and

using the modified representation to determine the dominant logic state (Page 439, CL1, Para 3).

Per Claim 2: **SI** teaches determining a plurality of partition groups each having two partitions by iteratively moving at least one node from the second partition to the first partition (Page 438, CL2, Para 2);

determining a partial logic state corresponding to each of the plurality of partition group(Page 438, CL2, Para 7); and

for each partial logic state, modifying the representation to determine at least one dominant. logic state (Page 438, CL2, Para 7 to Page 439, CL1, Para 1).

Per Claim 3: **SI** teaches that the at least one node is not the second power supply node (Page 438, CL2, Para 2).

Per Claim 4: **SI** teaches modifying the representation includes at least one of removing edges and merging nodes according to known inputs of the partial logic state (Page 438, CL2, Para 5).

Per Claim 5: **SI** teaches determining a first set of feasible inputs for each partial logic stat (Page 438, CL2, Para 7 to Page 439, CL1, Para 1; Fig 3); wherein:

if the first set is empty, enumerating states of the unknown inputs whose edges remain in the representation after modifying the representation to determine the at least one dominant logic state (Page 438, CL2, Para 7 to Page 439, CL1, Para 1; Fig 3); and

if the first set is not empty, updating the partial logic states based on the feasible inputs (Page 438, CL2, Para 7 to Page 439, CL1, Para 1; Fig 3).

Per Claim 6: **SI** teaches if the first set is not empty, modifying the graph representation and determining a second set of feasible inputs after updating the partial logic states (Page 438, CL2, Para 7 to Page 439, CL1, Para 1; Fig 3).

Per Claim 7: **SI** teaches enumerating is performed to determine a plurality of dominant logic states (Page 439, CL1, Para 3).

Per Claim 8: **SI** teaches the dominant logic state corresponds to a transistor within the integrated circuit that sees a drain-to-source voltage of the first power supply when the transistor is off (Page 438, CL1, Para 5 to Para 7).

Per Claim 9: **SI** teaches that the representation is a graph representation comprising nodes and edges (Page 438, CL2, Fig 3).

Per Claim 10: **SI** teaches that modifying the graph representation includes at least one of removing edges and merging nodes according to known inputs of the partial state (Page 437, CL2, Para 4).

Per Claim 11: **SI** teaches that the integrated circuit is a DC-connected component (DCC) (Page 437, CL2, Para 1; CL2, Para 3).

9.2 As per claim 12, **SI** teaches a method for determining a leakage current of an integrated circuit (Page 439, CL1, Para 6); comprising:

partitioning the integrated circuit into at least one DC-connected component (DCC) (Page 438, CL2, Fig 3);

determining a dominant logic state corresponding to the at least one DCC (Page 439, CL1, Para 3); and

calculating a leakage current for the at least one DCC corresponding to the dominant logic state (Page 439, CL1, Para 6; Table 2).

Per Claim 13: **SI** teaches determining is further characterized as determining a set of dominant logic states corresponding to the at least one DCC (Page 439, CL1, Para 3).

Per Claim 14: **SI** teaches calculating comprises calculating a leakage current corresponding to each dominant logic state within the set of dominant logic states (Page 439, CL1, Para 6; Table 2).

Per Claim 15: **SI** teaches the DCC includes at least one input (Page 437, CL2, Para 3), the method further comprising:

determining a probability corresponding to the at least one input; and using the probability and the leakage current to calculate an average DCC leakage current (Page 437, CL2, Para 3).

Per Claim 16: **SI** teaches the integrated circuit is partitioned into a plurality of DCCs, each DCC including at least one input (Page 438, CL2, Fig 3), the method further comprising:

determining a set of dominant logic states corresponding to each of the plurality of DCCs (Page 439, CL1, Para 3);

calculating a leakage current corresponding to each dominant logic state within each set of dominant logic states (Page 439, CL1, Para 6; Table 2);

determining a probability corresponding to the at least one input of each DCC (Page 437, CL2, Para 3);

using the corresponding probability and the corresponding leakage current to calculate an average DCC leakage current for each DCC (Page 437, CL2, Para 3); and

calculating an average circuit leakage for the integrated circuit using the average DCC leakage currents (Page 441, CL1, table 3; Page 440, CL2, Para7).

Per Claim 17: **SI** teaches the integrated circuit is partitioned into a plurality of DCCs (Page 438, CL2, Fig 3), the method further comprising:

determining a set of dominant logic states corresponding to each of the plurality of DCCs (Page 439, CL1, Para 3);

calculating a leakage current corresponding to each dominant logic state within each set of dominant logic states (Page 439, CL1, Para 6; Table 2); and

calculating an average circuit leakage for the integrated circuit (Page 441, CL1, table 3; Page 440, CL2, Para7).

Per Claim 18: **SI** teaches the at least one DCC is coupled to a first power supply (Page 438, CL2, Para 2; Fig 3); and

the dominant logic state corresponds to a transistor within the DCC that sees a drain-to-source voltage of the first power supply when the transistor is off (Page 438, CL1, Para 5 to Para 7).

Per Claim 19: **SI** teaches determining the dominant logic state corresponding to the at least one DCC (Page 439, CL1, Para 3) comprises:

using a representation of the DCC to determine a first partition and a second partition wherein the first partition includes a first power supply node and the second partition includes a second power supply node (Page 438, CL1, Fig 2; CL2, Fig 3; CL1, Para 3; CL2, Para 2);

determining a partial logic state corresponding to the first and second partitions (Page 438, CL1, Fig 2; CL2, Para 7);

modifying the representation according to the partial logic state (Page 438, CL2, Para 7); and

using the modified representation to determine the dominant logic state (Page 439, CL1, Para 3).

Per Claim 20: **SI** teaches calculating the leakage current for the at least one DCC corresponding to the dominant logic state (Page 439, CL1, Para 6; Table 2) comprises:

constructing a graph having nodes and edges according to the dominant logic state of the integrated circuit (Page 438, CL2, Fig 3);

calculating a leakage for each transistor in a first set of transistors (Page 439, CL1, Para 6);

modifying the graph based on the first set of transistors (Page 438, CL2, Fig 3);

calculating a leakage for each transistor in a second set of transistors (Page 439, CL1, Para 6); and

calculating the leakage current for the at least one DCC using the leakages for the transistors in the first set of transistors and the leakages for the transistors in the second set of transistors (Page 441, CL1, Table 3).

9.3 As per claim 21, **SI** teaches a method of improving performance of an integrated circuit (Page 440, CL1, Para 2 and 3), comprising:

for each transistor of the integrated circuit having a first threshold voltage level, calculating a first value based at least in part on delay and leakage corresponding to a second threshold voltage level (Page 440, CL1, Para 3), wherein calculating the first value comprises:

partitioning the integrated circuit into at least one DC-connected component (DCC) (Page 438, CL2, Fig 3);

determining a dominant logic state corresponding to the at least one DCC (Page 439, CL1, Para 3); and

calculating a leakage current for the at least one DCC corresponding to the dominant logic state (Page 441, CL1, table 3; Page 440, CL2, Para7);

selecting one of the transistors of the integrated circuit based on the first values (Page 440, CL2, Para 2);

setting the selected one of the transistors to the second threshold voltage level (Page 440, CL1, Para 3); and

modifying an area of at least one transistor within the integrated circuit (Page 440, CL1, Para 3).

Per Claim 22: **SI** teaches determining a cone of influence of the selected one of the transistors wherein the at least one transistor is within the cone of influence (Page 440, CL2, Para 4).

Per Claim 23: **SI** teaches that the selected one of the transistors and the at least one transistor is a same transistor (Page 440, CL2, Para 4).

Per Claim 24: **SI** teaches modifying includes modifying an area of each transistor within the cone of influence (Page 440, CL2, Para 4).

Per Claim 25: **SI** teaches sizing the integrated circuit to a predetermined area after modifying the area of the at least one transistor (Page 440, CL2, Para 5).

Per Claim 26: **SI** teaches determining a cone of influence of the selected one of the transistors, wherein modifying includes modifying an area of each transistor within the cone of influence (Page 440, CL2, Para 4).

Per Claim 27: **SI** teaches the integrated circuit has a first area prior to calculating the first values and the predetermined area approximately equals the first area (Page 440, CL2, Para 5).

Per Claim 28: **SI** teaches determining a circuit performance (Page 440, CL2, Para 5); and

if the circuit performance is below a predetermined performance level, repeating calculating the first values, selecting one of the transistors, setting the selected one of the transistors, modifying the area of the at least one transistor, and sizing the integrated circuit (Page 441, CL1, Table 4).

Per Claim 29: **SI** teaches determining a circuit performance (Page 440, CL2, Para 5); and

if the circuit performance is below a predetermined performance level, repeating calculating the first values, selecting one of the transistors, setting the selected one of the transistors (Page 441, CL1, Table 4), and modifying the area of the at least one transistor (Page 440, CL1, Para 3).

9.4 As per claim 31, **SI** teaches an improved integrated circuit manufactured using the method of claim 21 (Page 440, CL1, Para 3).

9.5 As per claim 32, **SI** teaches a method for calculating a leakage current of an integrated circuit (Page 441, CL1, table 3; Page 440, CL2, Para7), comprising:

constructing a graph having nodes and edges according to a dominant logic state of the integrated circuit (Page 438, CL2, Fig 3);

calculating a leakage for each transistor in a first set of transistors (Page 439, CL1, Para 6);

modifying the graph based on the first set of transistors (Page 438, CL2, Fig 3); and

calculating a leakage for each transistor in a second set of transistors (Page 439, CL1, Para 6).

Per Claim 33: **SI** teaches that the integrated circuit is a DC-connected component (DCC) (Page 437, CL2, Para 1; CL2, Para 3).

Per Claim 34: **SI** teaches that constructing the graph comprises modifying the graph according to a dominant logic state of the integrated circuit (Page 438, CL1, Para 5 to CL2, Para 2; Fig 3).

Per Claim 35: **SI** teaches that the first set of transistors includes transistors of the integrated circuit that are off and are coupled to both a first power supply node and a ground node (Page 438, CL2, Para 2; CL1, Para 5 and 6).

Per Claim 36: **SI** teaches that calculating the leakage for each transistor in the first set of transistors is performed using a lookup table (Page 439, CL1, Para 6).

Per Claim 37: **SI** teaches that calculating the leakage for each transistor in the second set of transistors comprises calculating a node voltage and using a lookup table (Page 439, CL1, Para 6).

Per Claim 38: **SI** teaches that modifying the graph includes removing from the graph an edge corresponding to each of the transistors in the first set of transistors (Page 438, CL2, Para 5).

Per Claim 39: **SI** teaches that the first set of transistors and the second set of transistors are mutually exclusive (Page 438, CL2, Para 2).

Per Claim 40: **SI** teaches calculating a leakage current of the integrated circuit by summing the leakages for the transistors in the first set and the leakages for the transistors in the second set (Page 439, CL1, Para 6).

9.6 As per claim 41, **SI** teaches a computer readable medium (Page 441, CL1, Para 1),, comprising:

a first plurality of instructions for receiving a representation of an integrated circuit (Page 438, CL1, Fig 2; CL2, Fig 3; CL1, Para 3; CL2, Para 2);

a second plurality of instructions for determining a first partition and a second partition wherein the first partition includes a first power supply node and the second partition includes a second power supply node(Page 438, CL1, Fig 2; CL2, Fig 3; CL1, Para 3; CL2, Para 2);

a third plurality of instructions for determining a partial logic state corresponding to the first and second partitions(Page 438, CL1, Fig 2; CL2, Para 7);

a fourth plurality of instructions for modifying the representation according to the partial logic state (Page 438, CL2, Para 7); and

a fifth plurality of instructions for using the modified representation to determine the dominant logic state (Page 439, CL1, Para 3).

9.7 As per claim 42, **SI** teaches a computer readable medium (Page 441, CL1, Para 1), comprising:

a first plurality of instructions for partitioning an integrated circuit into at least one DC-connected component (DCC) (Page 438, CL2, Fig 3);

a second plurality of instructions for determining a dominant logic state corresponding to the at least one DCC (Page 439, CL1, Para 3); and

a third plurality of instructions for calculating a leakage current for the at leas tone DCC corresponding to the dominant logic state (Page 439, CL1, Para 6; Table 2).

9.8 As per claim 43, **SI** teaches a computer readable medium (Page 441, CL1, Para 1), for analyzing an integrated circuit having a plurality of transistors, each of the plurality of transistors having a first threshold voltage level (Page 440, CL1, Para 2 and 3), comprising:

a first plurality of instructions for calculating a first value based at least in part on delay and leakage corresponding to a second voltage level for each of the plurality of transistors (Page 440, CL1, Para 3), wherein calculating the first value comprises:

partitioning the integrated circuit into at least one DC-connected component (DCC) (Page 438, CL2, Fig 3);

determining a dominant logic state corresponding to the at least one DCC (Page 439, CL1, Para 3); and

calculating a leakage current for the at least one DCC corresponding to the dominant logic state (Page 439, CL1, Para 6; Table 2);

a second plurality of instructions for selecting one of the plurality of transistors based on the first values (Page 440, CL2, Para 2);

a third plurality of instructions for setting the selected one of the transistors to the second threshold voltage (Page 440, CL1, Para 3); and

a fourth plurality of instructions for determining a cone of influence of the selected one of the transistors (Page 440, CL2, Para 4).

9.9 As per claim 44, **SI** teaches a computer readable medium (Page 441, CL1, Para 1), comprising:

a first plurality of instructions for receiving a graph having nodes and edges according to a dominant logic state of an integrated circuit (Page 438, CL2, Fig 3);

a second plurality of instructions for calculating a leakage for each transistor in a first set of transistors (Page 439, CL1, Para 6);

a third plurality of instructions for modifying the graph based on the first set of transistors (Page 438, CL2, fig 3); and

a fourth plurality of instructions for calculating a leakage for each transistor in a second set of transistors (Page 439, CL1, Para 6).

Conclusion

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 703-305-0043. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska, can be reached on (703) 305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

K. Thangavelu
Art Unit 2123
March 12, 2004

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER